# Pizzabox Memory

## Memory allocation

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| Parameter in C | Value | Comment |
| XPAR\_DDR3\_SDRAM\_MPMC\_BASEADDR  XPAR\_MPMC\_0\_MPMC\_BASEADDR | 0x4000 0000 | DDR3\_SDRAM |
| XPAR\_DDR3\_SDRAM\_MPMC\_HIGHADDR  XPAR\_MPMC\_0\_MPMC\_HIGHADDR | 0x7FFF FFFF |
| XPAR\_DDR3\_SDRAM\_SDMA\_CTRL\_BASEADDR | 0x8460 0000 |
| XPAR\_DDR3\_SDRAM\_SDMA\_CTRL\_HIGHADDR | 0x8460 FFFF |
| XPAR\_DDR3\_SDRAM\_MPMC\_CTRL\_BASEADDR | 0xFFFF FFFF |
| PQUEST\_CH0\_DDR\_OFFSET  np\_burst\_0::wr\_buf\_start\_addr | 0x5000 0000 |  |
| np\_burst\_0::wr\_buf\_length | 0x0800 0000 |  |
| PQUEST\_CH1\_DDR\_OFFSET  np\_burst\_1::wr\_buf\_start\_addr | 0x58000000 |  |
| np\_burst\_1::wr\_buf\_length | 0x0800 0000 |  |
| PQUEST\_CH2\_DDR\_OFFSET  np\_burst\_2::wr\_buf\_start\_addr | 0x6000 0000 |  |
| np\_burst\_2::wr\_buf\_length | 0x0800 0000 |  |
| PQUEST\_CH3\_DDR\_OFFSET  np\_burst\_3::wr\_buf\_start\_addr | 0x6800 0000 |  |
| np\_burst\_3::wr\_buf\_length | 0x0800 0000 |  |
| IO\_SCAN\_0\_DDR\_OFFSET  npi\_burst\_io::wr\_buf\_start\_addr | 0x7000 0000 |  |
| npi\_burst\_io::wr\_buf\_length | 0x0000 0FFF |  |
| STDIN\_BASEADDRESS | 0x8400 0000 |  |
| STDOUT\_BASEADDRESS | 0x8400 0000 |  |
| XPAR\_UARTLITE\_0\_BASEADDR | 0x8440 0000 | MDM\_0 |
| XPAR\_UARTLITE\_0\_HIGHADDR | 0x8440 FFFF |
| XPAR\_UARTLITE\_1\_BASEADDR | 0x8400 0000 | XPS\_UARTLITE\_0 |
| XPAR\_UARTLITE\_1\_HIGHADDR | 0x8400 FFFF |
| XPAR\_XPS\_IIC\_EEPROM\_BASEADDR  XPAR\_IIC\_0\_BASEADDR | 0x8410 0000 | XPS\_IIC\_EEPROM |
| XPAR\_XPS\_IIC\_EEPROM\_HIGHADDR  XPAR\_IIC\_0\_HIGHADDR | 0x8410 FFFF |
| XPAR\_IO\_CONF\_0\_BASEADDR | 0x8480 0000 | IO\_CONF\_0 |
| XPAR\_IO\_CONF\_0\_HIGHADDR | 0x8480 FFFF |
| XPAR\_ENC\_0\_BASEADDR | 0x8500 0000 | ENC\_0 |
| XPAR\_ENC\_0\_HIGHADDR | 0x8500 FFFF |
| XPAR\_ENC\_1\_BASEADDR | 0x8510 0000 | ENC\_1 |
| XPAR\_ENC\_1\_HIGHADDR | 0x8510 FFFF |
| XPAR\_ENC\_2\_BASEADDR | 0x8520 0000 | ENC\_2 |
| XPAR\_ENC\_2\_HIGHADDR | 0x8520 FFFF |
| XPAR\_ENC\_3\_BASEADDR | 0x8530 0000 | ENC\_3 |
| XPAR\_ENC\_3\_HIGHADDR | 0x8530 FFFF |
| XPAR\_ENC\_DUMMY\_0\_BASEADDR | 0x8550 0000 | ENC\_DUMMY\_0 |
| XPAR\_ENC\_DUMMY\_0\_HIGHADDR | 0x8550 FFFF |
| XPAR\_ENC\_DUMMY\_1\_BASEADDR | 0x8560 0000 | ENC\_DUMMY\_1 |
| XPAR\_ENC\_DUMMY\_1\_HIGHADDR | 0x8560 FFFF |
| XPAR\_ENC\_DUMMY\_2\_BASEADDR | 0x8570 0000 | ENC\_DUMMY\_2 |
| XPAR\_ENC\_DUMMY\_2\_HIGHADDR | 0x8570 FFFF |
| XPAR\_ENC\_DUMMY\_3\_BASEADDR | 0x8580 0000 | ENC\_DUMMY\_3 |
| XPAR\_ENC\_DUMMY\_3\_HIGHADDR | 0x8580 FFFF |
| XPAR\_EVR\_DUMMY\_0\_BASEADDR | 0x8590 0000 | EVR\_DUMMY\_0 |
| XPAR\_EVR\_DUMMY\_0\_HIGHADDR | 0x8590 FFFF |
| XPAR\_EVR\_0\_BASEADDR | 0x8600 0000 | EVR\_0 |
| XPAR\_EVR\_0\_HIGHADDR | 0x8600 FFFF |
| XPAR\_EVR\_0\_MEM0\_BASEADDR | 0x8610 0000 |
| XPAR\_EVR\_0\_MEM0\_HIGHADDR | 0x8610FFFF |
| XPAR\_EVR\_0\_MEM1\_BASEADDR | 0x86200000 |
| XPAR\_EVR\_0\_MEM1\_HIGHADDR | 0x8620FFFF |
| XPAR\_EVR\_0\_MEM2\_BASEADDR | 0x86300000 |
| XPAR\_EVR\_0\_MEM2\_HIGHADDR | 0x8630FFFF |
| XPAR\_PULSEGEN\_0\_BASEADDR | 0x86400000 | PULSEGEN\_0 |
| XPAR\_PULSEGEN\_0\_HIGHADDR | 0x8640FFFF |
| XPAR\_IO\_SCAN\_0\_BASEADDR | 0x86500000 | IO\_SCAN\_0 |
| XPAR\_IO\_SCAN\_0\_HIGHADDR | 0x8650FFFF |
| XPAR\_FLASH\_MEM0\_BASEADDR | 0x90000000 |  |
| XPAR\_FLASH\_MEM0\_HIGHADDR | 0x97FFFFFF |  |
| DDR3\_NPI0 | 0xC2000000 |  |
| DDR3\_NPI1 | 0xD0000000 |  |

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| baseaddr\_lut | |
| mod\_num | Value |
| **0** | **XPAR\_ENC\_0\_BASEADDR** |
| **1** | **XPAR\_ENC\_1\_BASEADDR** |
| **2** | **XPAR\_ENC\_2\_BASEADDR** |
| **3** | **XPAR\_ENC\_3\_BASEADDR** |
| 4 | XPAR\_ENC\_DUMMY\_0\_BASEADDR |
| 5 | XPAR\_ENC\_DUMMY\_1\_BASEADDR |
| 6 | XPAR\_ENC\_DUMMY\_2\_BASEADDR |
| 7 | XPAR\_ENC\_DUMMY\_3\_BASEADDR |
| 8 | XPAR\_EVR\_DUMMY\_0\_BASEADDR |
| 9 | XPAR\_PULSEGEN\_0\_BASEADDR |
| 10 | XPAR\_IO\_CONF\_0\_BASEADDR |
| **11** | **XPAR\_IO\_SCAN\_0\_BASEADDR** |

## Memory operation

### Circular buffer operation (read in software).

Circular buffers are created in DDR3 SDRAM and are used to store Tx data for psc module ENC0~3 and IO\_SCAN. Each time 1024\*16 bytes (1024 data chunks) are read from the buffer and sent through network.

* Circular buffers are reset by setting tail🡨head. (Q: How is head/tail initialized?)
* Tail indicates the position from where read should start. Tail is stored in register 1 @(BASE\_ADDRESS + 4\*1) since the buffer is 4-byte wide. It is read at the beginning of each read, incremented and stored back into registered 1.
* Head is stored in register 5 @(BASE\_ADDRESS + 4\*5).
* Skip is stored in register 7 @(BASE\_ADDRESS + 4\*7).
* What are the other registers?